IN THE CLAIMS

This is a complete and current listing of the claims, marked with status identifiers in parentheses. The following listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

a data gate circuit that transmits a data gate signal;

a data circuit that transmits or receives data under control of the data gate signal;

a media gate circuit that transmits a media gate signal; and

a mode selection circuit that transmits mode selection information under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal~~; and~~

~~a buffer attention circuit that receives a buffer attention signal~~ .

2. (Original) The latency-independent interface of claim 1, wherein the mode selection information comprises tag information and control information.

3. (Original) The latency-independent interface of claim 2, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

4. (Original) The latency-independent interface of claim 3, wherein the control information further comprises a reset command.

5. (Original) The latency-independent interface of claim 3, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

6. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

a data gate circuit that receives a data gate signal;

a data circuit that transmits or receives data under control of the data gate signal;

a media gate circuit that receives a media gate signal; and

a mode selection circuit that receives mode selection information under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal ~~; and~~

~~a buffer attention circuit that transmits a buffer attention signal~~ .

7. (Original) The latency-independent interface of claim 6, wherein the mode selection information comprises tag information and control information.

8. (Original) The latency-independent interface of claim 7, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

9. (Original) The latency-independent interface of claim 8, wherein the control information further comprises a reset command.

10. (Original) The latency-independent interface of claim 8, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

11. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

a first data gate circuit that transmits a data gate signal;

a first data circuit that transmits or receives data under control of the data gate signal;

a first media gate circuit that transmits a media gate signal;

a first mode selection circuit that transmits mode selection information under control of the media gate signal;

~~a first buffer attention circuit that receives a buffer attention signal;~~

a second data gate circuit that receives the data gate signal;

a second data circuit that transmits or receives data under ~~the~~ control of the data gate signal;

a second media gate circuit that receives the media gate signal; and

a second mode selection circuit that receives mode selection information under control of the media gate signal~~; and a second buffer attention circuit that transmits the buffer attention signal~~ , wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal.

12. (Original) The latency-independent interface of claim 11, wherein the mode selection information comprises tag information and control information.

13. (Original) The latency-independent interface of claim 12, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

14. (Original) The latency-independent interface of claim 13, wherein the control information further comprises a reset command.

15. (Original) The latency-independent interface of claim 13, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

16. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

data gate circuit means for transmitting a data gate signal;

data circuit means for transmitting or receiving data under control of the data gate signal;

media gate circuit means for transmitting a media gate signal; and

mode selection circuit means for transmitting mode selection information under control of the media gate signal , wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal~~; and~~

~~buffer attention circuit means for receiving a buffer attention signal~~ .

17. (Original) The latency-independent interface of claim 16, wherein the mode selection information comprises tag information and control information.

18. (Original) The latency-independent interface of claim 17, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

19. (Original) The latency-independent interface of claim 18, wherein the control information further comprises a reset command.

20. (Original) The latency-independent interface of claim 18, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

21. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

data gate circuit means for receiving a data gate signal;

data circuit means for transmitting or receiving data under control of the data gate signal;

media gate circuit means for receiving a media gate signal; and

mode selection circuit means for receiving mode selection information under control of the media gate signal~~; and~~

~~buffer attention circuit means for transmitting a buffer attention signal~~ , wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal.

22. (Original) The latency-independent interface of claim 21, wherein the mode selection information comprises tag information and control information.

23. (Original) The latency-independent interface of claim 22, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

24. (Original) The latency-independent interface of claim 23, wherein the control information further comprises a reset command.

25. (Original) The latency-independent interface of claim 23, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

26. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

first data gate circuit means for transmitting a data gate signal;

first data circuit means for transmitting or receiving data under control of the data gate signal;

first media gate circuit means for transmitting a media gate signal,

first mode selection circuit means for transmitting mode selection information under control of the media gate signal;

~~first buffer attention circuit means for receiving a buffer attention signal;~~

second data gate circuit means for receiving the data gate signal;

second data circuit means for transmitting or receiving data under control of the data gate signal;

second media gate circuit means for receiving the media gate signal; and

second mode selection circuit means for receiving mode selection information under control of the media gate signal , wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal ~~; and~~

~~second buffer attention circuit means for transmitting a buffer attention signal~~ .

27. (Original) The latency-independent interface of claim 26, wherein the mode selection information comprises tag information and control information.

28. (Original) The latency-independent interface of claim 27, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

29. (Original) The latency-independent interface of claim 28, wherein the control information further comprises a reset command.

30. (Original) The latency-independent interface of claim 28, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

31. (Currently Amended) A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a data gate signal;

transmitting or receiving data under control of the data gate signal;

transmitting a media gate signal; and

transmitting mode selection information under the control of the media gate signal , wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal~~; and~~

~~receiving a buffer attention signal~~ .

32. (Original) The method of claim 31, wherein the mode selection information comprises tag information and control information.

33. (Original) The method of claim 32, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

34. (Original) The method of claim 33, wherein the control information further comprises a reset command.

35. (Original) The method of claim 33, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

36. (Currently Amended) A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a data gate signal;

transmitting or receiving data under control of the data gate signal;

receiving a media gate signal; and

receiving mode selection information under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware

components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal~~; and~~

~~transmitting a buffer attention signal~~.

37. (Original) The method of claim 36, wherein the mode selection information comprises tag information and control information.

38. (Original) The method of claim 37, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

39. (Original) The method of claim 38, wherein the control information further comprises a reset command.

40. (Original) The method of claim 38, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

41. (Currently Amended) A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting and receiving a data gate signal;

transmitting or receiving data under control of the data gate signal;

transmitting and receiving a media gate signal; and

transmitting and receiving mode selection information under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal~~; and~~

~~transmitting and receiving a buffer attention signal~~ .

42. (Original) The method of claim 41, wherein the mode selection information comprises tag information and control information.

43. (Original) The method of claim 42, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

44. (Original) The method of claim 43, wherein the control information further comprises a reset command.

45. (Original) The method of claim 43, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

46. (Currently Amended) An interface protocol between at least a first and second ~~two~~ hardware ~~components~~ component, comprising:

a transmitted data gate signal;

a data signal carrying data that is transmitted or received under control of the data gate signal;

a transmitted media gate signal; and

a mode selection signal carrying mode selection information that is transmitted under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal~~; and~~

~~a received buffer attention signal~~.

47. (Original) The interface protocol of claim 46, wherein the mode selection information comprises tag information and control information.

48. (Original) The interface protocol of claim 47, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

49. (Original) The interface protocol of claim 48, wherein the control information further comprises a reset command.

50. (Original) The interface protocol of claim 48, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

51. (Currently Amended) An interface protocol between at least a first and second ~~two~~ hardware ~~components~~ component, comprising:

a received data gate signal;

a data signal carrying data that is transmitted or received under control of the data gate signal;

a received a media gate signal; and

a mode selection signal carrying mode selection information that is received under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and at least one of the first and second hardware components in accordance with the media gate signal; ~~and~~

~~a transmitted buffer attention signal~~ .

52. (Original) The interface protocol of claim 51, wherein the mode selection information comprises tag information and control information.

53. (Original) The interface protocol of claim 52, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

54. (Original) The interface protocol of claim 53, wherein the control information further comprises a reset command.

55. (Original) The interface protocol of claim 53, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

56. (Currently Amended) An interface protocol between at least a first and second ~~two~~ hardware ~~components~~ component, comprising:

a data gate signal transmitted by ~~a~~ the first hardware component and received by ~~a~~ the second hardware component;

a data signal that transmits data between the first and second hardware components under control of the data gate signal;

a media gate signal transmitted by the first hardware component and received by the second hardware component; and

a mode selection signal that transmits mode selection information from the first hardware component to the second hardware component under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal~~; and~~

~~a buffer attention signal transmitted by the second hardware component and received by the first hardware component~~ .

57. (Original) The interface protocol of claim 56, wherein the mode selection information comprises tag information and control information.

58. (Original) The interface protocol of claim 57, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

59. (Original) The interface protocol of claim 58, wherein the control information further comprises a reset command.

60. (Original) The interface protocol of claim 58, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

61. (Currently Amended) A ~~device readable medium embodying a~~ program ~~of instructions~~ for execution by a device for performing a method of transmitting and receiving signals between first and second hardware components, the program ~~of instructions~~ comprising instructions for:

transmitting a data gate signal;

transmitting or receiving data under control of the data gate signal;

transmitting a media gate signal; and

transmitting mode selection information under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware

components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal; and

receiving a buffer attention signal .

62. (Currently Amended) The device readable medium of program of claim 61, wherein the mode selection information comprises tag information and control information.

63. (Currently Amended) The device readable medium of program of claim 62, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

64. (Currently Amended) The device readable medium of program of claim 63, wherein the control information further comprises a reset command.

65. (Currently Amended) The device readable medium of program of claim 63, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

66. (Currently Amended) A device readable medium embodying a program of instructions for execution by a device for performing a method of transmitting and receiving signals between first and second hardware components, the program of instructions comprising instructions for:

receiving a data gate signal;

transmitting or receiving data under control of the data gate signal;

receiving a media gate signal; and

receiving mode selection information under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware

components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal~~; and~~

~~transmitting a buffer attention signal~~.

67. (Currently Amended) The ~~device-readable medium of~~ program of claim 66, wherein the mode selection information comprises tag information and control information.

68. (Currently Amended) The ~~device-readable medium of~~ program of claim 67, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

69. (Currently Amended) The ~~device-readable medium of~~ program of claim 68, wherein the control information further comprises a reset command.

70. (Currently Amended) The ~~device-readable medium of~~ program of claim 68, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

71. (Currently Amended) A ~~device-readable medium embodying a~~ program ~~of instructions~~ for execution by a device for performing a method of transmitting and receiving signals between first and second hardware components, the program ~~of instructions~~ comprising instructions for:

transmitting and receiving a data gate signal;

transmitting or receiving data under control of the data gate signal;

transmitting and receiving a media gate signal; and

transmitting and receiving mode selection information under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and

second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal~~; and~~

~~transmitting and receiving a buffer attention signal~~.

72. (Currently Amended) The ~~device readable medium of~~ program of claim 71, wherein the mode selection information comprises tag information and control information.

73. (Currently Amended) The ~~device readable medium of~~ program of claim 72, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

74. (Currently Amended) The ~~device readable medium of~~ program of claim 73, wherein the control information further comprises a reset command.

75. (Currently Amended) The ~~device readable medium of~~ program of claim 73, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

76. (New) The latency-independent interface of claim 1, further comprising a buffer attention circuit that receives a buffer attention signal.

77. (New) The latency-independent interface of claim 6, further comprising a buffer attention circuit that transmits a buffer attention signal .

78. (New) The latency-independent interface of claim 11, further comprising a first buffer attention circuit that receives a buffer attention signal and a second buffer attention circuit that transmits the buffer attention signal.

79. (New) The latency-independent interface of claim 16, further comprising buffer attention circuit means for receiving a buffer attention signal .

80. (New) The latency-independent interface of claim 21, further comprising buffer attention circuit means for transmitting a buffer attention signal.

81. (New) The latency-independent interface of claim 26, further comprising first buffer attention circuit means for receiving a buffer attention signal and second buffer attention circuit means for transmitting a buffer attention signal .

82. (New) The method of claim 31, further comprising receiving a buffer attention signal .

83. (New) The method of claim 36, further comprising transmitting a buffer attention signal.

84. (New) The method of claim 41, further comprising transmitting and receiving a buffer attention signal .

85. (New) The interface protocol of claim 46, further comprising a received buffer attention signal.

86. (New) The interface protocol of claim 51, further comprising a transmitted buffer attention signal .

87. (New) The interface protocol of claim 56, further comprising a buffer attention signal transmitted by the second hardware component and received by the first hardware component .

88. (New) The program of claim 61, further comprising receiving a buffer attention signal .

89. (New) The program of claim 66, further comprising transmitting a buffer attention signal.

90. (New) The program of claim 71, further comprising transmitting and receiving a buffer attention signal.

91. (New) A device readable medium, comprising the program of claim 61.

92. (New) A device readable medium, comprising the program of claim 66.

93. (New) A device readable medium, comprising the program of claim 71.

94. (New) A first hardware component including a latency-independent interface for communication between the first and a second hardware component, comprising:

a data gate circuit that transmits a data gate signal;

a data circuit that transmits or receives data under control of the data gate signal;

a media gate circuit that transmits a media gate signal; and

a mode selection circuit that transmits mode selection information under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal.

95. (New) The hardware component of claim 94, wherein the mode selection information comprises tag information and control information.

96. (New) The hardware component of claim 95, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

97. (New) The hardware component of claim 96, wherein the control information further comprises a reset command.

98. (New) The hardware component of claim 96, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

99. (New) A first hardware component including a latency-independent interface for communication between the first and a second hardware component, comprising:

a data gate circuit that receives a data gate signal;

a data circuit that transmits or receives data under control of the data gate signal;

a media gate circuit that receives a media gate signal; and

a mode selection circuit that receives mode selection information under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the first hardware component in accordance with the media gate signal.

100. (New) The hardware component of claim 99, wherein the mode selection information comprises tag information and control information.

101. (New) The hardware component of claim 100, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

102. (New) The hardware component of claim 101, wherein the control information further comprises a reset command.

103. (New) The hardware component of claim 101, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

104. (New) An apparatus, comprising:

a first hardware component including a first interface, the first interface including,

a first data gate circuit that transmits a data gate signal,

a first data circuit that transmits or receives data under control of the data gate signal,

a first media gate circuit that transmits a media gate signal, and

a first mode selection circuit that transmits mode selection information under control of the media gate signal; and

a second hardware component including a second interface, the second interface including,

a second data gate circuit that receives the data gate signal,

a second data circuit that transmits or receives data under ~~the~~ control of the data gate signal,

a second media gate circuit that receives the media gate signal, and

a second mode selection circuit that receives mode selection information under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal.

105. (New) The apparatus of claim 104, wherein the mode selection information comprises tag information and control information.

106. (New) The apparatus of claim 105, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

107. (New) The apparatus of claim 106, wherein the control information further comprises a reset command.

108. (New) The apparatus of claim 106, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

109. (New) A first hardware component including a latency-independent interface for communication between the first and a second hardware component, comprising:

data gate circuit means for transmitting a data gate signal;

data circuit means for transmitting or receiving data under control of the data gate signal;

media gate circuit means for transmitting a media gate signal; and

mode selection circuit means for transmitting mode selection information under control of the media gate signal , wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal.

110. (New) The hardware component of claim 109, wherein the mode selection information comprises tag information and control information.

111. (New) The hardware component of claim 110, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

112. (New) The hardware component of claim 111, wherein the control information further comprises a reset command.

113. (New) The hardware component of claim 111, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

114. (New) A first hardware component including a latency-independent interface for communication between the first and a second hardware component, comprising:

data gate circuit means for receiving a data gate signal;

data circuit means for transmitting or receiving data under control of the data gate signal;

media gate circuit means for receiving a media gate signal; and

mode selection circuit means for receiving mode selection information under control of the media gate signal, wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the first hardware component in accordance with the media gate signal.

115. (New) The hardware component of claim 114, wherein the mode selection information comprises tag information and control information.

116. (New) The hardware component of claim 115, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

117. (New) The hardware component of claim 116, wherein the control information further comprises a reset command.

118. (New) The hardware component of claim 116, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

119. (New) An apparatus, comprising:

a first hardware component including a first interface, the first interface including,

first data gate circuit means for transmitting a data gate signal,

first data circuit means for transmitting or receiving data under control of the data gate signal,

first media gate circuit means for transmitting a media gate signal, and

first mode selection circuit means for transmitting mode selection information under control of the media gate signal; and

a second hardware component including a second interface, the second interface including,

second data gate circuit means for receiving the data gate signal,

second data circuit means for transmitting or receiving data under control of the data gate signal,

second media gate circuit means for receiving the media gate signal, and

second mode selection circuit means for receiving mode selection information under control of the media gate signal , wherein said data gate signal controls the transfer of data between the first and second hardware components and wherein data is transferred between a storage media and the second hardware component in accordance with the media gate signal.

120. (New) The apparatus of claim 119, wherein the mode selection information comprises tag information and control information.

121. (New) The apparatus of claim 120, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

122. (New) The apparatus of claim 121, wherein the control information further comprises a reset command.

123. (New) The apparatus of claim 121, wherein the control information further comprises size information comprising a size command that indicates size of associated data.